PATENT ABSTRACTS OF JAPAN

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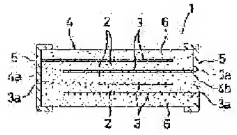
(54) LAMINATION TYPE SEMICONDUCTOR CERAMIC ELEMENT



(57)Abstract:
PURPOSE: To acquire a lamination type semiconductor ceramic element which can reduce a resistance value at a room temperature without damaging ohmic characteristic and can increase a resistance variation ratio.
CONSTITUTION: A semiconductor ceramic layer 2 and an electrode 3 are laminated alternately and a lamination 4 (sintered body) is formed. When a lamination type semiconductor ceramic element 1 is thereby constituted, porosity of the ceramic element 1 is made 3 to 15vol.%.

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CLAIMS

[Claim(s)]

[Claim 1] The laminating mold semi-conductor ceramic component characterized by making voidage of this semi-conductor ceramic component into three to 15 volume % in the laminating mold semi-conductor ceramic component which has the forward resistance temperature characteristic which comes to carry out the laminating of a semi-conductor ceramic layer and the electrode by turns.

[Claim 2] The laminating mold semi-conductor ceramic component characterized by the above-mentioned electrode containing at least one or more kinds of elements among nickel, Cu, Fe, Co, W, Ta, Ti, and Mo in claim 1.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the structure which could be made to enlarge resistance rate of change while being able to make resistance low, without an electric resistance value spoiling the ohmic nature of an electrode in a detail about the laminating mold semi-conductor ceramic component which has the forward resistance temperature characteristic which changes with temperature.
[0002]
[Description of the Prior Art] The barium titanate system semiconductor device which has a forward resistance temperature characteristic has the property which resistance increases rapidly above the Curie point, for example, is used for many applications, such as an overcurrent-protection component of an electrical circuit, or a demagnetization component of the Braun-tube frame of television. Moreover, in recent years, the laminating mold semi-conductor ceramic component which can respond to a surface mount and can make the resistance in a room temperature small is proposed (for example, refer to JP,55-88304,A and JP,57-60802,A). This laminating mold semiconductor device is BaTiO3. The laminating of the internal electrode which consists of a semi-conductor ceramic layer used as a principal component and a Pt-Pd alloy is carried out by turns, and it is really sintered.
[0003]
[Problem(s) to be Solved by the Invention] However, in the above-mentioned conventional laminating mold semiconductor device, when metals, such as Pt and Pd, are adopted as an internal electrode, since the Schottky barrier arises between this electrode and a ceramic layer, ohmic contact is hard to be acquired, and there is a problem that it is inferior to the stability of resistance as a result.

[0004] Here, in order to acquire ohmic contact, it is possible to adopt small nickel of a work function etc. as an internal electrode. In this case, in order to avoid oxidation of nickel, once carrying out elevated-temperature baking in a reducing atmosphere and sintering, it is made to perform reoxidation processing at the temperature which is extent to which Above nickel does not oxidize this sintered compact. However, since the conditioning in the case of performing this reoxidation processing is difficult, the problem of being easy to produce unevenness is in oxidation treatment. Consequently, if oxidation is weak, the surface section and inside a sintered compact, resistance will differ and the problem that resistance rate of change becomes small as a result will produce the surface part of a sintered compact from oxidation not going to the interior, although it oxidizes. [which were obtained] If the above-mentioned oxidation is strong, since oxidation will go to the interior of a sintered compact, although resistance rate of change is made greatly on the other hand, the problem that an internal electrode oxidizes and ohmic nature is spoiled arises. For this reason, in the present condition, it has become difficult to obtain a component with large resistance rate of change low [room temperature resistance], and the improvement at this point is demanded.

[0005] This invention was made in view of the above-mentioned conventional situation, and it aims at offering the laminating mold semi-conductor ceramic component which can enlarge resistance rate of change while being able to make the resistance in a room temperature low, without spoiling the ohmic nature in the case of performing reoxidation processing using nickel.

[0006]

[Means for Solving the Problem] Preventing oxidation of an electrode, when [which should find out the approach of oxidizing to the interior of a sintered compact] it inquires wholeheartedly, by forming the opening section in a ceramic component, these artificers hit on an idea for oxidation conditions to be controlled, as a result for oxidation unevenness to be prevented, and accomplish this invention.

[0007] Then, this invention is characterized by making voidage of this semi-conductor ceramic component into three to 15 volume % in the laminating mold semi-conductor ceramic component which comes to carry out the laminating of a semi-conductor ceramic layer and the conductive layer by turns.

[0008] Regulating the range of the above-mentioned voidage here because oxidation would not progress and the improvement effect of resistance rate of change would not be acquired, if it was made to 3% or less, it

is because there is a possibility that it may become easy to produce oxidation of an internal electrode, and the anti-chip box reinforcement of a sintered compact may moreover be fallen and damaged when the 15 above-mentioned% is exceeded.
[0009] Moreover, in order to form the opening section in the above-mentioned ceramic component, it is realizable by carrying out addition mixing of the resin powder burned down at the time of baking. To the above-mentioned internal electrode, it is still more desirable to contain at least one or more kinds of elements among nickel, Cu, Fe, Co, W, Ta, Ti, and Mo from which ohmic contact is acquired.
[0010]
[Function] Since according to the laminating mold semi-conductor ceramic component concerning this invention the opening section was formed in this ceramic component and this voidage was specified, oxidation can be promoted to the interior of a sintered compact, avoiding the oxidation to the internal electrode in the case of performing reoxidation processing, and the unevenness of oxidation can be prevented. Consequently, while being able to make the resistance in a room temperature low, without spoiling ohmic contact, resistance rate of change can be enlarged and it can respond to an above-mentioned request.
[0011]
[Example] Hereafter, the example of this invention is explained about drawing. Drawing 1 and drawing 2 are drawings for explaining the laminating mold semi-conductor ceramic component by one example of this invention.
[0012] In drawing, 1 is the laminating mold semi-conductor ceramic component of this example. This ceramic component 1 is a rectangular parallelepiped-like thing, and is BaTiO3. The laminating of the semi-conductor ceramic layer 2 used as a principal component and the internal electrode 3 which consists of nickel is carried out by turns, and it is constituted by the sintered compact 4 which really comes to sinter this layered product. After this sintered compact 4 carries out elevated-temperature baking of the layered product in a reducing atmosphere, in atmospheric air, it performs reoxidation processing and is obtained.
[0013] End side 3a of each above-mentioned internal electrode 3 is the left of a sintered compact 4, It is exposed to the right end sides 4a and 4b by turns, and each remaining end face is located inside the ceramic layer 2, and is laid underground in the sintered compact 4. Moreover, left of the above-mentioned sintered compact 4, The external electrodes 5 and 5 which consist of Ag are formed in the right end sides 4a and 4b, and end side 3a of each above-mentioned internal electrode 3

is electrically connected to this external electrode 5.
[0014] And the opening section which is not illustrated is formed in the above-mentioned semi-conductor ceramic component 1, and the voidage of this has become 3 - 15 volume %. This opening section mixes resin powder into a ceramic ingredient, in case it calcinates this, it is made burned down, and it is formed.
[0015] Next, the 1 manufacture approach of the laminating mold semi-conductor ceramic component 1 of this example is explained. First, they are BaCO3, SrCO3, CaCO3, TiO2, La 2O3, SiO2, and MnCO3 as a raw material. It prepares so that it may use and may become the following presentations.
(Ba0.857 calcium0.10Sr0.04La0.003) TiO3+0.008 Mn+0.01SiO2 [0016] After paying the above-mentioned raw material to the pot made from polyethylene with pure water and a zirconia ball and carrying out grinding mixing for 5 hours, it is made to dry and temporary baking is carried out at 1100 degrees C for 2 hours. Subsequently, this temporary baking object is pulverized and temporary baking powder is formed.
[0017] And an organic binder, a solvent, and a dispersant are mixed into the above-mentioned temporary baking powder, and a mean diameter is 10 micrometers to this. A polystyrene particle is added and it mixes. It is made for this polystyrene particle to become within the limits of 3 - 15 volume % to the above-mentioned ceramic ingredient. 50 micrometers in the slurry obtained by this to thickness A ceramic green sheet is fabricated and it is 7.5x6.6mm about this green sheet. It cuts in the shape of a rectangle, and many semi-conductor ceramic layers 2 and the ceramic layer 6 for dummies are formed.
[0018] Next, the electric conduction powder and varnish which consist of nickel are mixed, electrode paste is created, this paste is printed on the top face of each above-mentioned semi-conductor ceramic layer 2, and an internal electrode 3 is formed. When printing this internal electrode 3, only end side 3a of this is prolonged to the rim of the ceramic layer 2, and other end faces are formed so that it may be located inside.
[0019] And as shown in drawing 2 , the above-mentioned semi-conductor ceramic layer 2 and an internal electrode 3 lap by turns, and end side 3a of each internal electrode 3 is the left of the ceramic layer 2, It piles up so that it may be located in a right end side by turns, and the ceramic layer 6 for dummies is further put on the upper part of this, and the lower part. This is stuck by pressure with a press and a layered product is formed.
[0020] Subsequently, the above-mentioned layered product is heated at 1300 degrees C in the reducing atmosphere of H2 / 2 = 3% of N, and is

calcinated for 2 hours, and a sintered compact 4 is obtained. Then, reoxidation processing is performed for this sintered compact 4 by 800 ** in atmospheric air for 2 hours. Then, oxygen will permeate the opening section of this and a sintered compact 4 will oxidize to the interior of this.

[0021] To the last, it is the left of the above-mentioned sintered compact 4, After applying Ag paste to the right end sides 4a and 4b, it can be burned and the external electrode 5 is formed. Thereby, the laminating mold semi-conductor ceramic component 1 of this example is manufactured.

[0022] It can oxidize up to the sintered compact 4 interior, preventing oxidation of the internal electrode 3 in the case of performing reoxidation processing, since according to the laminating mold semi-conductor ceramic component 1 of this example the opening section was formed in the semi-conductor ceramic component 1 and voidage was made into 3 - 15%. Consequently, without spoiling the ohmic nature of the above-mentioned internal electrode 3, low [room temperature resistance], a component with large resistance rate of change can be obtained, and it can respond to an above-mentioned request.

[0023] In addition, in the above-mentioned example, although nickel was adopted as the internal electrode, this invention is effective in adopting Cu, Fe, Co, W, Ta, Ti, and Mo, and the same ohmic nature as the above-mentioned example being obtained also in this case.

[0024]

[Table 1]

空隙率とＰＴＣ特性、および焼結体の抗折強度

試料番号	空隙率（体積％）	室温抵抗 at25℃（Ω）	抵抗変化率 ρ250/ρ25	抗折強度（kg/cm^2）
＊ 1	1．6	0．4	11	689
＊ 2	2．8	0．8	83	643
3	3．0	1．4	1430	632
4	4．9	2．4	1820	558
5	8．2	3．5	4670	511
6	11．3	5．6	5260	459
7	12．6	6．6	6330	447
8	15．0	9．8	6820	338
＊ 9	15．3	36．2	8170	127
＊10	19．4	84．8	7290	81

[0025] Table 1 shows the result of the characteristic test which checks the effectiveness of this example and which went to accumulate. This trial adds a polystyrene particle into an above-mentioned ceramic ingredient, changed the addition of this, changed the voidage of the semi-conductor ceramic component 1 in 1.6 - 19.4% of range, and created sample No.1-10. and -- this -- each -- the resistance (omega) in the room temperature of sample No.1-10, and resistance rate of change, And anti-chip box reinforcement (Kg/cm2) It measured. In addition, front Naka and * mark show the outside of the range of this invention. Moreover, the above-mentioned resistance rate of change was computed by the degree type.

resistance rate-of-change =(2.303/T2-T1) x100T1: -- temperature T2: from which resistance will be the room temperature resistance [10 times] -- 100 of room temperature resistance of resistance Doubling temperature

[0026] When voidage is 3% or less of sample No.1, and 2 so that clearly also from Table 1, although room temperature resistance is low,

resistance rate of change is as small as 11 and 83 %, and oxidation of a ceramic is not progressing. moreover -- although a value with large resistance rate of change is acquired in the case of sample No.9 which made voidage 15% or more, and 10 -- oxidation of an internal electrode -- room temperature resistance -- 36. -- 2 and 84.8 It is high with omega and, moreover, anti-chip box reinforcement is falling rapidly with 127 and 81 kg/cm2. On the other hand, in the case of this example sample No.3-8 which made voidage 3 - 15% of within the limits, for any sample, room temperature resistance is 1.4-9.8. The value with as large resistance rate of change as 1430 - 6820% is low acquired with omega. Furthermore, anti-chip box reinforcement is 632 - 338 kg/cm2. It is high and the satisfying value is acquired.

[0027]

[Effect of the Invention] According to the laminating mold semi-conductor ceramic component which starts this invention as mentioned above, since voidage of this ceramic component was made into 3 - 15% of range, it is effective in the ability to obtain a component with large resistance rate of change low [room temperature resistance], without spoiling ohmic nature.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is a sectional view for explaining the laminating mold semi-conductor ceramic component by one example of this invention.

[Drawing 2] It is the decomposition perspective view of the semi-conductor ceramic component of the above-mentioned example.

[Description of Notations]

1 Laminating Mold Semi-conductor Ceramic Component

2 Semi-conductor Ceramic Layer
3 Internal Electrode
4 Sintered Compact (Layered Product)

[Translation done.]

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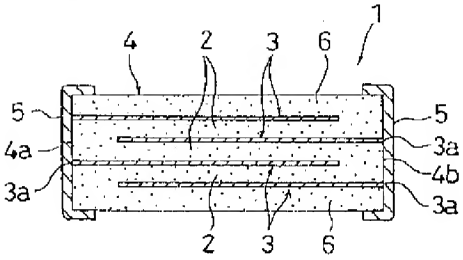
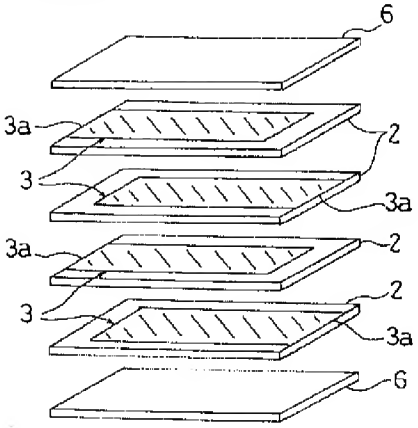
DRAWINGS

[Drawing 1]



[Drawing 2]



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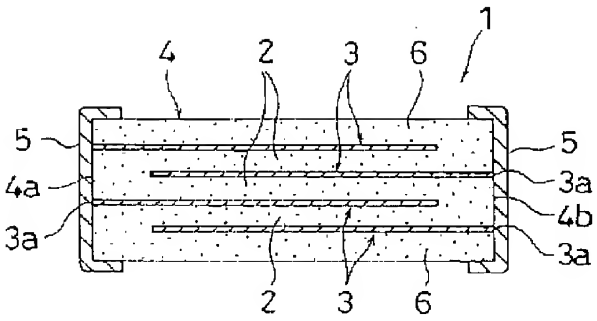
(54)【発明の名称】　積層型半導体セラミック素子

(57)【要約】
【目的】　オーミック性を損なうことなく室温での抵抗値を低くできるとともに、抵抗変化率を大きくできる積層型半導体セラミック素子を提供する。
【構成】　半導体セラミック層２と電極３とを交互に積層して積層体４（焼結体）を形成し、これにより積層型半導体セラミック素子１を構成する場合に、該セラミック素子１の空隙率を３～１５体積％とする。



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【特許請求の範囲】

【請求項１】　半導体セラミック層と電極とを交互に積層してなる正の抵抗温度特性を有する積層型半導体セラミック素子において、該半導体セラミック素子の空隙率を３～１５体積％としたことを特徴とする積層型半導体セラミック素子。

【請求項２】　請求項１において、上記電極がＮｉ，Ｃｕ，Ｆｅ，Ｃｏ，Ｗ，Ｔａ，Ｔｉ，Ｍｏのうち少なくとも１種類以上の元素を含んでいることを特徴とする積層型半導体セラミック素子。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、電気抵抗値が温度によって変化する正の抵抗温度特性を有する積層型半導体セラミック素子に関し、詳細には電極のオーミック性を損なうことなく抵抗値を低くできるとともに、抵抗変化率を大きくできるようにした構造に関する。

【０００２】

【従来の技術】正の抵抗温度特性を有するチタン酸バリウム系半導体素子は、キュリー点以上で抵抗値が急激に増加する特性を有しており、例えば電気回路の過電流保護素子、あるいはテレビのブラウン管枠の消磁素子など多くの用途に利用されている。また、近年では表面実装に対応でき、かつ室温での抵抗値を小さくできる積層型半導体セラミック素子が提案されている（例えば、特開昭５５－８８３０４号公報，特開昭５７－６０８０２号公報参照）。この積層型半導体素子は、$BaTiO_3$ を主成分とする半導体セラミック層とＰｔ－Ｐｄ合金からなる内部電極とを交互に積層して一体焼結したものである。

【０００３】

【発明が解決しようとする課題】しかしながら上記従来の積層型半導体素子では、内部電極にＰｔ，Ｐｄ等の金属を採用すると、該電極とセラミック層との間でショットキー障壁が生じることからオーミック接触が得られ難く、その結果抵抗値の安定性に劣るという問題がある。

【０００４】ここで、オーミック接触を得るためには、内部電極に仕事関数の小さいＮｉ等を採用することが考えられる。この場合、Ｎｉの酸化を回避するために還元性雰囲気にて高温焼成して一旦焼結した後、該焼結体を上記Ｎｉが酸化されない程度の温度で再酸化処理を行うようにしている。ところが、この再酸化処理を行う場合の条件設定が困難であることから、酸化処理にむらが生じ易いという問題がある。その結果、酸化が弱いと焼結体の表面部分は酸化されるものの内部まで酸化が進まないことから、得られた焼結体の表面部と内部とでは抵抗値が異なり、その結果抵抗変化率が小さくなるという問題が生じる。一方、上記酸化が強いと焼結体内部まで酸化が進むことから抵抗変化率は大きくできるものの、内部電極が酸化されてオーミック性が損なわれるという問題が生じる。このため現状では室温抵抗値の低い、かつ抵抗変化率の大きい素子を得ることが困難となっており、この点での改善が要請されている。

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【０００５】本発明は上記従来の状況に鑑みてなされたもので、Ｎｉを用いて再酸化処理を行う場合の、オーミック性を損なうことなく室温での抵抗値を低くできるとともに、抵抗変化率を大きくできる積層型半導体セラミック素子を提供することを目的としている。

【０００６】

【課題を解決するための手段】本件発明者らは、電極の酸化を防止しながら焼結体内部まで酸化できる方法を見出すべき鋭意検討したところ、セラミック素子に空隙部を形成することによって酸化条件を制御でき、ひいては酸化むらを防止できることに想到し、本発明を成したものである。

【０００７】そこで本発明は、半導体セラミック層と導電層とを交互に積層してなる積層型半導体セラミック素子において、該半導体セラミック素子の空隙率を３～１５体積％としたことを特徴としている。

【０００８】ここで、上記空隙率の範囲を規制したのは、３％以下にすると酸化が進まなくなり、抵抗変化率の改善効果が得られないからであり、上記１５％を越えると内部電極の酸化が生じ易くなり、しかも焼結体の抗折強度が低下して破損するおそれがあるからである。

【０００９】また、上記セラミック素子に空隙部を形成するには、例えば焼成時に焼失する樹脂粉末等を添加混合することにより実現できる。さらに上記内部電極には、オーミック接触が得られるＮｉ，Ｃｕ，Ｆｅ，Ｃｏ，Ｗ，Ｔａ，Ｔｉ，Ｍｏのうち少なくとも１種類以上の元素を含有することが好ましい。

【００１０】

【作用】本発明に係る積層型半導体セラミック素子によれば、該セラミック素子に空隙部を形成し、該空隙率を規定したので、再酸化処理を行う場合の内部電極への酸化を回避しながら焼結体内部まで酸化を促進でき、かつ酸化のむらを防止できる。その結果、オーミック接触を損なうことなく室温での抵抗値を低くできるとともに、抵抗変化率を大きくでき、上述の要請に応えられる。

【００１１】

【実施例】以下、本発明の実施例を図について説明する。図１及び図２は本発明の一実施例による積層型半導体セラミック素子を説明するための図である。

【００１２】図において、１は本実施例の積層型半導体セラミック素子である。このセラミック素子１は直方体状のもので、$BaTiO_3$ を主成分とする半導体セラミック層２と、Ｎｉからなる内部電極３とを交互に積層し、この積層体を一体焼結してなる焼結体４により構成されている。この焼結体４は、積層体を還元性雰囲気にて高温焼成した後、大気中にて再酸化処理を施して得られたものである。

【００１３】上記各内部電極３の一端面３ａは焼結体４の左，右端面４ａ，４ｂに交互に露出されており、残りの各端面はセラミック層２の内側に位置して焼結体４内に埋設されている。また上記焼結体４の左，右端面４ａ，４ｂにはＡｇからなる外部電極５，５が形成されており、この外部電極５に上記各内部電極３の一端面３ａが電気的に接続されている。

【００１４】そして、上記半導体セラミック素子１には図示しない空隙部が形成されており、これの空隙率は３～１５体積％となっている。この空隙部はセラミック材料に樹脂粉末を混合し、これを焼成する際に焼失させて形成されたものである。

【００１５】次に、本実施例の積層型半導体セラミック素子１の一製造方法について説明する。まず、原料として、$BaCO_3$，$SrCO_3$，$CaCO_3$，TiO_2，La_2O_3，SiO_2，$MnCO_3$ を用いて以下の組成となるよう調合する。

$(Ba_{0.857}Ca_{0.10}Sr_{0.04}La_{0.003})TiO_3 + 0.008\ Mn + 0.01SiO_2$

【００１６】上記原料を純水及びジルコニアボールとともにポリエチレン製ポットに入れて５時間粉砕混合した後、乾燥させて1100℃で２時間仮焼成する。次いでこの仮焼成体を粉砕して仮焼成粉を形成する。

【００１７】そして、上記仮焼成粉に、有機バインダ，溶剤，及び分散剤を混合し、これに平均粒径が10μｍのポリスチレン粒子を添加して混合する。このポリスチレン粒子は上記セラミック材料に対して３～１５体積％の範囲内となるようにする。これにより得られたスラリーから厚さ50μｍのセラミックグリーンシートを成形し、このグリーンシートを7.5×6.6㎜の矩形状にカットして多数の半導体セラミック層２とダミー用セラミック層６を形成する。

【００１８】次に、Ｎｉからなる導電粉末とワニスとを混合して電極ペーストを作成し、このペーストを上記各

半導体セラミック層２の上面に印刷して内部電極３を形成する。この内部電極３を印刷する場合、これの一端面３ａのみがセラミック層２の外縁まで延び、他の端面は内側に位置するように形成する。

【００１９】そして、図２に示すように、上記半導体セラミック層２と内部電極３とが交互に重なり、かつ各内部電極３の一端面３ａがセラミック層２の左，右端面に交互に位置するように重ね、さらにこれの上部，下部にダミー用セラミック層６を重ねる。これをプレスで圧着して積層体を形成する。

【００２０】次いで、上記積層体を、$H_2/N_2 = 3\%$ の還元性雰囲気中で1300℃に加熱して２時間焼成し、焼結体４を得る。この後、この焼結体４を大気中にて800℃で２時間再酸化処理を行う。すると焼結体４はこれの空隙部に酸素が浸透し、該内部まで酸化されることとなる。

【００２１】最後に、上記焼結体４の左，右端面４ａ，４ｂにＡｇペーストを塗布した後、焼き付けて外部電極５を形成する。これにより本実施例の積層型半導体セラミック素子１が製造される。

【００２２】本実施例の積層型半導体セラミック素子１によれば、半導体セラミック素子１に空隙部を形成し、かつ空隙率を３～１５％としたので、再酸化処理を行う場合の内部電極３の酸化を防止しながら、焼結体４内部まで酸化することができる。その結果、上記内部電極３のオーミック性を損なうことなく、室温抵抗値の低い、かつ抵抗変化率の大きい素子を得ることができ、上述の要請に応えられる。

【００２３】なお、上記実施例では、内部電極にＮｉを採用したが、本発明はＣｕ，Ｆｅ，Ｃｏ，Ｗ，Ｔａ，Ｔｉ，Ｍｏを採用してもよくこの場合も上記実施例と同様のオーミック性が得られる効果がある。

【００２４】

【表１】

5　　6

空隙率とＰＴＣ特性、および焼結体の抗折強度

試料番号	空隙率（体積%）	室温抵抗 at25℃（Ω）	抵抗変化率 ρ250/ρ25	抗折強度（kg/cm²）
＊ 1	1．6	0．4	11	689
＊ 2	2．8	0．8	83	643
3	3．0	1．4	1430	632
4	4．9	2．4	1820	558
5	8．2	3．5	4670	511
6	11．3	5．6	5260	459
7	12．6	6．6	6330	447
8	15．0	9．8	6820	338
＊ 9	15．3	36．2	B170	127
＊10	19．4	84．8	7290	81

【００２５】表１は、本実施例の効果を確認するために行った特性試験の結果を示す。この試験は、上述のセラミック材料にポリスチレン粒子を添加し、これの添加量を変化させて半導体セラミック素子１の空隙率を1.6 ～19.4%の範囲で変化させて試料No．１～１０を作成した。そしてこの各試料No．１～１０の室温での抵抗値（Ω），抵抗変化率，及び抗折強度（ Kg/cm² ）を測定した。なお、表中、＊印は本発明の範囲外を示す。また上記抵抗変化率は次式により算出した。

抵抗変化率＝（2.303 ／Ｔ２－Ｔ１）×100

Ｔ１：抵抗が室温抵抗の10倍になる温度

Ｔ２：抵抗が室温抵抗の100 倍になる温度

【００２６】表１からも明らかなように、空隙率が３％以下の試料No．１，２の場合は、室温抵抗値は低いものの、抵抗変化率が11,83 %と小さく、セラミックの酸化が進んでいない。また空隙率を１５％以上とした試料No．９，１０の場合は、抵抗変化率は大きい値が得られるものの、内部電極の酸化により室温抵抗値が36.2,84.8 Ωと高くなっており、しかも抗折強度は127,81Kg/cm²と急激に低下している。これに対して空隙率を３～１５%の範囲内とした本実施例試料No．３～８の場合、何れの試料も室温抵抗値は1.4 ～9.8 Ωと低く、また抵抗変化率は1430～6820%と大きい値が得られている。さらに抗折強度は632 ～338Kg/cm² と高く、満足できる値が得られている。

【００２７】

【発明の効果】以上のように本発明に係る積層型半導体セラミック素子によれば、該セラミック素子の空隙率を３～１５％の範囲としたので、オーミック性を損なうことなく室温抵抗値の低い、かつ抵抗変化率の大きい素子を得ることができる効果がある。

【図面の簡単な説明】

【図１】本発明の一実施例による積層型半導体セラミック素子を説明するための断面図である。

【図２】上記実施例の半導体セラミック素子の分解斜視図である。

【符号の説明】

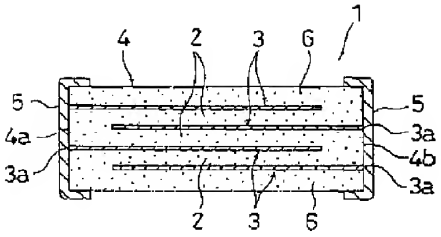
1　積層型半導体セラミック素子

2　半導体セラミック層

3　内部電極

4　焼結体（積層体）

【図１】



【図２】